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DESIGN AND ANALYSIS OF MUX USING ADIABATIC TECHNIQUES ECRL AND PFAL

Thiyagu S[1], **Bathri Prasath R**[2] **Mothis K**[3], **Sheik Abdul Kadar M S Y**[4],,
[1]*Student, Dept. of Electronics Communication Engineering, Bannari Amman Institute of Technology, IN*
[2]*Student, Dept. of Electronics Communication Engineering, Bannari Amman Institute of Technology, IN*
[3]Student, Dept. of *Electronics Communication Engineering*, Bannari Amman Institute of Technology, IN
[4]Student, Dept. of *Electronics Communication Engineering*, Bannari Amman Institute of Technology, IN

Abstract - *The design and analysis of a multiplexer (Mux) circuit utilizing adiabatic switching techniques, specifically focusing on Energy Recovery Logic (ERL) and Charge Recovery Logic (CRL), with particular emphasis on the ECRL and PFAL families. The primary objective is to significantly reduce power dissipation by recovering energy during signal transitions, which would otherwise be dissipated as heat in conventional CMOS circuits. Adiabatic logic circuits achieve this by performing logic transitions at slow voltage rates, allowing for energy recovery through controlled voltage sources or inductive elements. This study investigates methods to maximize the energy recovery, optimizing the inclusion of components like inductors and capacitors to facilitate energy transfer, minimize losses, and enhance efficiency.*

A key challenge is to maintain an optimal balance between slow voltage transitions—required for energy recovery—and the need for acceptable switching speeds that meet the requirements of modern digital systems. We present a design for an efficient adiabatic multiplexer that incorporates these principles, ensuring that the circuit is capable of low power operation while meeting performance constraints. Simulations are conducted to assess various metrics, including power consumption, energy recovery efficiency, and switching speed, and to validate the effectiveness of adiabatic switching techniques in real-world scenarios.

Key Words: Energy Charge Recovery logic (ECRL),Positive Feedback Adiabatic Logic(PFAL), Adiabatic Logic.

1. INTRODUCTION

The demand for portable and mobile electronic devices continues to rise, the need for low-power, high-performance circuits has become increasingly critical. These devices—ranging from smartphones and wearables to sensors and Internet of Things (IoT) devices—are highly dependent on energy efficiency to extend battery life and minimize heat dissipation. Power dissipation inconventional digital circuits, particularly dynamic power consumption during switching, has become one of the primary barriers to achieving greater energy efficiency. In traditional CMOS (Complementary Metal-Oxide-Semiconductor) circuits, energy is dissipated in the form of heat primarily due to charging and discharging of capacitances, which occurs every time a logic transition happens. This results in a significant energy loss, especially as operating frequencies increase and circuit density grows.

The digital systems operating at high frequencies, the energy spent in switching transistors from one logic state to another becomes substantial. Furthermore, as technology nodes shrink and transistor sizes decrease, leakage currents and static power dissipation also become a concern. In such an environment, energy-efficient circuit design is no longer optional but essential, especially in applications where power is a limited resource, such as battery-powered devices and embedded systems.

1.1 Adiabatic Logic Circuits: The Concept of Energy Recovery

Adiabatic logic circuits operate on the principle of performing logic transitions through slow voltage changes that allow the circuit to recover and reuse energy that would otherwise be lost as heat. The key to these circuits is the "adiabatic" process, where the switching speed is carefully controlled so that the energy stored in the capacitive load during a logic transition is not wasted but returned to the power supply. In this way, the amount of energy dissipated during the switching event is minimized, leading to a drastic reduction in power consumption compared to conventional CMOS circuits, which dissipate most of the energy as heat.

In typical digital circuits, a significant amount of energy is consumed by the charging and discharging of capacitive nodes, which leads to dynamic power dissipation. In contrast, adiabatic circuits use specialized techniques such as controlled voltage sources and inductive components to transfer energy efficiently between the circuit and the power supply, minimizing energy loss. These circuits operate with

slow transitions to ensure that voltage changes are gradual enough to allow for the recovery of energy, making them a promising solution for reducing the overall energy consumption in digital systems.

One of the major challenges, however, is to ensure that these slow transitions do not excessively degrade the performance of the system. Adiabatic circuits tend to introduce latency in switching operations, as slower voltage transitions inherently lead to longer switching times. Therefore, it is critical to find a balance between achieving low power consumption and maintaining acceptable performance, especially in high-speed or high-performance applications where switching speed is paramount.

1.2 Energy Recovery Logic (ERL) and Charge Recovery Logic (CRL)

Among the different types of adiabatic logic families, Energy Recovery Logic (ERL) and Charge Recovery Logic (CRL) are two of the most well-known. These families are based on the principle of energy recovery, where the energy used in switching logic states is returned to the power supply for reuse. Unlike conventional CMOS circuits, which dissipate energy as heat, ERL and CRL circuits allow for a significant portion of the energy to be recovered.

Energy Recovery Logic (ERL), for example, typically uses controlled voltage sources to regulate the voltage during switching transitions, allowing energy to be transferred efficiently between the power supply and the circuit elements. The key advantage of ERL is that it enables the energy used in the switching process to be stored and returned to the power source, greatly reducing the energy lost during transitions.

A more specific subset of ERL is Charge Recovery Logic (CRL), which focuses on recovering the charge stored in capacitors during switching events. CRL circuits are designed to carefully manage the voltage waveforms in such a way that the energy stored in the capacitive nodes is retrieved and returned to the power supply, rather than being wasted as heat. CRL techniques are particularly effective in low-power applications and can lead to significant power savings when applied to logic circuits.

These adiabatic logic families have gained attention due to their potential to lower power dissipation in digital circuits. However, the implementation of adiabatic logic is not without its challenges. While energy recovery is a key benefit, there is a need for precise control of voltage waveforms and careful management of transition speeds to avoid performance degradation. Slow voltage transitions can increase latency, which may not be acceptable in many high-performance systems.

2. OBJECTIVE

2.1 Achieve Lower Power Dissipation:

Design an adiabatic multiplexer circuit that minimizes power consumption by utilizing adiabatic switching techniques, specifically ECRL and PFAL, which enable energy recovery during logic transitions and reduce heat dissipation compared to conventional CMOS circuits.

2.2 Maximize Energy Recovery:

Maximize the recovery of energy that would otherwise be dissipated as heat during logic transitions by incorporating energy-recovery mechanisms, such as inductors or controlled voltage sources, within the multiplexer design to optimize the reuse of energy.

2.3 Balance Power Efficiency and Switching Speed:

Ensure that the adiabatic multiplexer design achieves a balance between the slow voltage transitions required for energy recovery and the acceptable switching speed needed for practical applications in digital systems, ensuring that performance is not compromised.

2.3 Optimize Circuit Performance via Simulation::

Perform extensive simulations of the adiabatic multiplexer circuit to evaluate its energy recovery efficiency, power dissipation, and switching speed, and to compare the performance of the proposed design with traditional CMOS-based multiplexers.

2.3 Integrate Adiabatic Circuit Techniques for Practical Applications:

Implement adiabatic logic design techniques, suchas ECRL and PFAL, within the multiplexer circuit to improve power efficiency while ensuring that the design is feasiblefor integration with modern semiconductor manufacturing technologies and meets required performance standards.

3. PROPOSED SYSTEM

3.1 Overview of the Proposed System

The proposed system aims to design a low-power multiplexer using adiabatic switching techniques, specifically Energy Recovery Logic (ECRL) and Positive Feedback Adiabatic Logic (PFAL). By employing these energy-efficient techniques, the multiplexer will recover energy during logic transitions, thus minimizing power dissipation and reducing heat generation, while maintaining acceptable switching speeds and performance. This approach is ideal for digital circuits in battery-powered devices, Internet of Things (IoT) devices, wearable electronics, and high-performance low-power systems, where energy efficiency and long battery life are crucial.

Unlike traditional CMOS multiplexers, which suffer from high dynamic power dissipation due to capacitive charging and discharging, the proposed adiabatic multiplexer uses controlled slow voltage transitions to ensure that the energy dissipated during logic transitions is recovered and reused, instead of being lost as heat. This system aims to achieve a significant reduction in energy consumption without compromising on the necessary functionality and speed of the multiplexer.

3.2 Energy Charge Recovery Logic (ECRL) Multiplexer:

ECRL is a subtype of Energy Charge Recovery Logic that uses a charge-recovery mechanism to allow the energy used in logic transitions to be efficiently stored and returned to the power supply.

In the proposed multiplexer, ECRL is used to ensure that energy is recovered during each logic transition by employing slow voltage transitions and controlled charging/discharging of capacitive nodes.

The energy recovered from the output and intermediate nodes is fed back to the power supply or other parts of the circuit, thus improving the overall power efficiency.

3.2 Positive Feedback Adiabatic Logic (PFAL):

PFAL is another adiabatic logic style that uses a feedback mechanism to regulate the voltage and current during the switching process. The positive feedback ensures that the voltage change occurs gradually and in a controlled manner, which helps in minimizing energy loss.

PFAL circuits maintain voltage levels for longer periods during transitions, which facilitates energy recovery and minimizes the loss of power during signal transitions.

In the multiplexer, PFAL is employed in conjunction with ECRL to further optimize the switching process, ensuring that both energy recovery and performance are balanced.

3.3 Controlled Voltage Sources

The proposed system will integrate controlled voltage sources and possibly inductive components to store and release energy as needed. These components are used to manage the slow voltage transitions and allow for energy recovery during switching cycles.

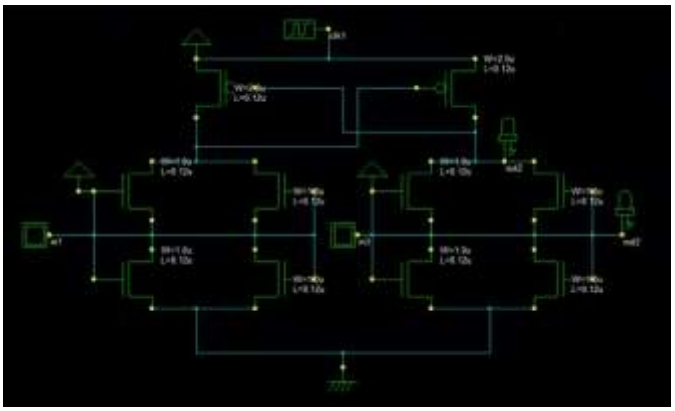
The controlled voltage sources are responsible for ensuring that voltage transitions are slow enough to recover energy efficiently but fast enough to ensure the multiplexer operates within acceptable timing limits.

3.4 Low-Voltage Operation:

The adiabatic multiplexer will operate at lower supply voltages, further reducing power consumption. Adiabatic techniques, particularly in energy recovery, are well-suited for low-voltage designs because they rely on slow transitions rather than the rapid voltage changes used in traditional logic.

4 Circuit Diagram :

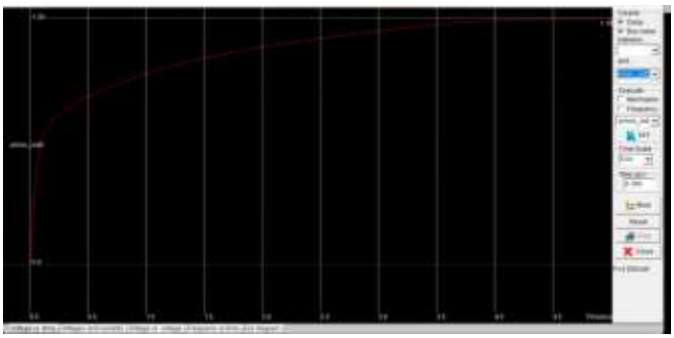
4.1 Circuit Diagram of ECRL



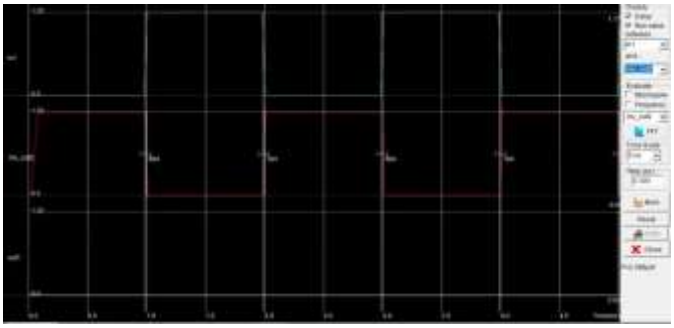
4.2 Circuit Diagram of PFAL

5 Output:

5.1 ECRL output with power



5.2 PFAL output with power



6 Conclusion:

The project focused on the design and analysis of a multiplexer (Mux) using adiabatic switching techniques, specifically Energy-Recovery Logic (ECRL) and Positive Feedback Adiabatic Logic (PFAL), to achieve lower power dissipation and enhance energy recovery during signal transitions. By leveraging these techniques, we successfully demonstrated how energy typically lost as heat in conventional CMOS designs can be recovered, leading to significant power savings without compromising circuit functionality.

Through simulation and analysis, we showed that adiabatic multiplexers offer a promising solution for low-power digital systems. The use of ECRL and PFAL not only reduced dynamic power consumption but also maintained functional performance with acceptable switching speeds. These techniques proved to be effective in recovering energy during circuit transitions, addressing the growing need for energy-efficient designs in modern electronics, particularly in battery-powered and IoT devices.

The project confirmed that adiabatic logic techniques like ECRL and PFAL are viable options for energy-efficient VLSI design. The proposed multiplexer design is scalable and can be integrated into larger systems, making it ideal for future applications in low-power processors, sensor networks, and mobile devices. Future work can explore more complex applications and further optimizations, including integration with larger digital systems and adaptation to smaller process nodes, ensuring the relevance of these techniques in advancing energy-efficient electronics.

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